

FREQUENCY SPECTRUM COMPRESSION/EXPANSION APPARATUS

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- **international:** G10L21/04; G11C27/00; H04B1/66; G10L21/00; G11C27/00; H04B1/66; (IPC1-7): G10L1/00; G11C27/00; H04B1/66

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DE3320888 (A1)

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Abstract not available for JP58216300

Abstract of corresponding document: [DE3320888](#)

This device contains a number of analog shift registers, a clock generator for a successive phase-shifted execution of the writing-in and reading-out of the analog shift registers, a gate or multiplier circuit through which only the read-out signal from each analog shift register is passed, a squarewave signal generator for generating a squarewave signal which controls the opening and closing of the gate circuit, in which radio-frequency components of the squarewave signal are removed so that rising edges and falling edges of the squarewave signal are smoothed and a monotonic rise and fall of the read-out signal output by the gate circuit is obtained, as a result of which interference on the connecting part between the read-out output signals of the individual analog shift registers is avoided.

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